JAPANESE [JP,2001-274201,A]

CLAIMS DETAILED DESCRIPTION TECHNICAL FIELD PRIOR ART EFFECT OF THE INVENTION TECHNICAL PROBLEM MEANS DESCRIPTION OF DRAWINGS DRAWINGS

[Translation done.]

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DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Field of the Invention]This invention relates to a suitable electron device for inter-electrode low-temperature degree junction, and a manufacturing method for the same about an electron device and a manufacturing method for the same.
[0002]
[Description of the Prior Art]As a semiconductor device which can be comparatively manufactured by low cost with a thin shape, there are a semiconductor device which adopts tape automated bonding (only henceforth TAB) structure, and a semiconductor device which adopts flip chip (only henceforth FC) structure.
[0003]The semiconductor device which adopts TAB structure is provided with a semiconductor device (semiconductor chip) and a flexible tape substrate, and is constituted. For example between the bonding pad (electrode) of a semiconductor device, and the lead of a tape substrate, a gold bump electrode is made to intervene, and it is connected electrically and mechanically by thermocompression bonding.
[0004]On the other hand, the semiconductor device which adopts FC structure is similar with the semiconductor device which adopts TAB structure.
It has a semiconductor device and a tape substrate and is constituted.
A semiconductor device is mounted so that it may face each other on the surface of a tape substrate in the element formation side, for example, a gold bump electrode is made to intervene between the bonding pad of a semiconductor device, and the lead wire on a tape substrate, and it is connected electrically and mechanically by thermocompression bonding.
[0005]
[Problem(s) to be Solved by the Invention]In each of the semiconductor device which adopts the above-mentioned TAB structure, and the semiconductor device which adopts FC structure, consideration was not made about the following points.
[0006]Around about 500 ** high temperature is used for the bonding pad of a semiconductor device, the lead of a tape substrate, or thermocompression bonding with a lead wire. For this reason, the tape substrate which heat resistance is required of the tape substrate which uses resin as the main ingredients, and has heat resistance is expensive. Therefore, the semiconductor device as a final product had the problem of becoming expensive.
[0007]This invention is made in order to solve an aforementioned problem. Therefore, the purpose of this invention is to provide the electron device which has a joinable electrode in the degree of low temperature.
[0008]The purpose of this invention is to provide the electron device which can decrease product cost by use of the parts which do not need heat resistance, material, etc.
[0009]The purpose of this invention is to provide the electron device whose joined part of an electrode

Drawing selection
Representative draw.

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can be electric and which can improve the bonding strength of an electrode, and can improve mechanical reliability.

[0010]The purpose of this invention is to provide the manufacturing method of the electron device which can make inter-electrode junction the degree of low temperature.

[0011]The purpose of this invention is to provide the manufacturing method of the electron device which can decrease a manufacturing cost.

[0012]

[Means for Solving the Problem]In order to solve an aforementioned problem, the 1st feature of this invention, An electrode which has a liquid phase diffusion metal in a surface layer at least, and the 1st metal layer for junction it is allocated on this electrode and combined with a liquid phase diffusion metal, the 2nd junction that is allocated on the 1st metal layer for junction, and lowers combination temperature of a liquid phase diffusion metal and the 1st metal layer for junction -- public funds -- it is having considered it as an electron device provided with a group.

[0013]Here, it is used in a meaning which contains an electronic device, electronic parts, or a mounting device built combining them with a "electron device." For example, a semiconductor device, a resistance element, a capacitative element, etc. are contained in an electronic device. A substrate, a lead, a package, etc. are included in electronic parts. A device which mounted two or more semiconductor devices in a package or a substrate, for example, a semiconductor module, a mounting board, etc. are contained in a mounting device. With "an electrode which has a liquid phase diffusion metal in a surface layer at least", an electrode in which the whole was formed with a liquid phase diffusion metal, and an electrode which has a liquid phase diffusion metal in a part of surface layer are used in a meaning included at least. With an "electrode", it is used in a meaning of an electric connection terminal for inputting, outputting, or outputting and inputting current and voltage, and a single electrode, an electrode of wiring, an electrode of a lead, etc. are contained in this "electrode" at least. An electrode connected to other electrodes inside an electron device and an electrode connected to other electrodes of the exterior (for example, other electron devices and devices) of an electron device are used for an "electrode" in a meaning included at least.

[0014]in an electron device concerning the 1st feature of this invention, "liquid phase diffusion metal" of the melting point is lower than this liquid phase diffusion metal -- "-- the 1st junction -- public funds -- if group" is fused, isothermal solidification of the counter diffusion will be produced and carried out between metal which should be joined, and it will be used in a meaning of metal which generates a liquid-phase-diffusion-welding layer. Copper (Cu), gold (Au), aluminum (aluminum), nickel (nickel), ceramics ($aluminum_2O_3$), etc. are contained in this "liquid phase diffusion metal" at least.

[0015]duality which makes the main ingredients tin (Sn), lead (Pb), indium (In), or one of them at "the 1st metal layer for junction" -- the above alloy is contained at least. "-- duality of the 1st metal layer for junction -- quaternary alloys, such as ternary alloys, such as binary alloys, such as In-Ag, In-Sn, Bi-Sn, Bi-Pb, and Bi-In, In-Pb-Ag, and Bi-Sn-Pb, and Bi-In-Pb-Sn, are contained in alloy" of a more than, for example. Of course, a 5 yuan or more alloy is contained in "the 1st metal layer for junction."

[0016]"Combination temperature of a liquid phase diffusion metal and the 1st metal layer for junction is lowered" of the 2nd metal layer for junction is used for the purpose of lowering liquid phase diffusion temperature of a liquid phase diffusion metal, i.e., melting temperature of a liquid phase diffusion metal and the 1st metal layer for junction. duality which makes the main ingredients bismuth (Bi), silver (Ag), In, or one of them at least at "the 2nd metal layer for junction" -- the above alloy is contained. this -- "-- duality -- alloy" of a more than -- "-- duality of the 1st metal layer for junction -- it is used in the same meaning as alloy" of a more than, and is used in a meaning in which a ternary alloy, a quaternary alloy, and a 5 yuan or more alloy are contained.

[0017]In an electron device concerning the 1st feature of this invention constituted in this way, welding temperature by liquid phase diffusion between an electrode and other electrodes connected to it -- the 2nd junction -- public funds -- lowering by a group -- moreover -- bonding strength between both sides -- the 2nd junction -- public funds -- since a group can raise, heat-resistant temperature which builds this electron device, such as parts and material, can be lowered. Therefore, since costs, such as these parts and material, can be reduced, product cost of an electron device is reducible. Since a low-temperature degree process is employable in a manufacturing process of an electron device, product cost of an electron device can be reduced further.

[0018]In an electron device concerning the 1st feature of this invention, the 2nd feature of this invention is having used a liquid phase diffusion metal as a rolling thin film. Here, a "rolling thin film" is used for a liquid phase diffusion metal at least in a meaning which says a thin film which performed a rolling process. This "rolling thin film" is a thin film which has the character recrystallized in the range with a particle diameter of 1 micrometer - 20 micrometers in the degree of low temperature which are 100 ** - 300 ** and in which particle diameter size becomes large compared with particle diameter of recrystallization of an "electrolysis thin film", for example, when Cu is used for a liquid

phase diffusion metal.
[0019]In an electron device concerning the 2nd feature of this invention constituted in this way, since particle diameter size of a liquid phase diffusion metal can be enlarged and a plane-of-composition product can be increased by having used a liquid phase diffusion metal as a rolling thin film, bonding strength of an electrode can be improved.
[0020]The 1st electrode to which the 3rd feature of this invention has a liquid phase diffusion metal in a surface layer at least, a liquid phase diffusion metal and the 1st junction that this liquid phase diffusion metal is made to combine -- public funds -- a group and a liquid phase diffusion metal, and the 1st junction -- public funds -- the 2nd junction that lowers combination temperature with a group -- public funds -- it is having considered it as an electron device provided with a liquid-phase-diffusion-welding layer on the 1st electrode which contains a group at least, and the 2nd electrode on a liquid-phase-diffusion-welding layer.
[0021]here -- "a liquid-phase-diffusion-welding layer" -- the 2nd junction -- public funds -- in the state where combination temperature was lowered by a group -- at least -- a liquid phase diffusion metal of the 1st electrode, and the 1st junction -- public funds -- as a result of combining a group, it is used in a meaning of a generated joining layer. therefore, the main ingredients of a "liquid-phase-diffusion-welding layer" -- a liquid phase diffusion metal and the 1st junction -- public funds -- it is a group -- "a liquid-phase-diffusion-welding layer" -- as the main ingredients -- the 2nd junction -- public funds -- it does not need to be contained even if a group is contained.
[0022]In an electron device concerning the 3rd feature of this invention constituted in this way, welding temperature by liquid phase diffusion between the 1st electrode and the 2nd electrode connected to it -- the 2nd junction -- public funds -- it lowering by a group and, moreover -- bonding strength between both sides -- the 2nd junction -- public funds -- since it can have a liquid-phase-diffusion-welding layer which can be raised by a group and between the 1st electrode and the 2nd electrode can be joined by this liquid-phase-diffusion-welding layer, heat-resistant temperature which builds this electron device, such as parts and material, can be lowered. Therefore, since costs, such as these parts and material, can be reduced, product cost of an electron device is reducible. Since a low-temperature degree process is employable in a manufacturing process of an electron device, product cost of an electron device can be reduced further.
[0023]A process in which the 4th feature of this invention forms the 1st electrode that has a liquid phase diffusion metal in a surface layer at least, the 1st junction combined with it on a liquid phase diffusion metal -- public funds -- with a process of forming a group. the 1st junction -- public funds -- a group top -- a liquid phase diffusion metal and the 1st junction -- public funds -- the 2nd junction that lowers combination temperature with a group -- public funds -- with a process of forming a group. the 2nd junction -- public funds -- a process of forming the 2nd electrode on a group, and the 2nd junction -- public funds -- a group -- a liquid phase diffusion metal and the 1st junction -- public funds -- it is having made a process of combining a group, forming a liquid-phase-diffusion-welding layer, and joining between the 1st electrode and the 2nd electrode into a manufacturing method of an electron device which it had at least.
[0024]in a manufacturing method of an electron device concerning the 4th feature of such this invention -- a liquid phase diffusion metal and the 1st junction -- public funds -- combination temperature with a group -- the 2nd junction -- public funds -- since it can lower by a group, inter-electrode welding temperature can be lowered and a low-temperature degree process can be realized.
[0025]A process in which the 5th feature of this invention forms the 1st electrode that has the 1st liquid phase diffusion metal in a surface layer at least, the 1st junction combined with it on the 1st liquid phase diffusion metal -- public funds -- with a process of forming a group. the 1st junction -- public funds -- a group top -- the 1st liquid phase diffusion metal and the 1st junction -- public funds -- the 2nd junction that lowers combination temperature with a group -- public funds -- with a process of forming a group. A process of forming the 2nd electrode that has the 2nd liquid phase diffusion metal in a surface layer at least, the 3rd junction combined with it on the 2nd liquid phase diffusion metal -- public funds -- with a process of forming a group. the 3rd junction -- public funds -- a group top -- the 2nd liquid phase diffusion metal and the 3rd junction -- public funds -- the 4th junction that lowers combination temperature with a group -- public funds -- a process of forming a group, and the 2nd junction -- public funds -- a group and the 4th junction -- public funds -- by a group. the 1st liquid phase diffusion metal and the 1st junction -- public funds -- combining a group -- and the 2nd liquid phase diffusion metal and the 3rd junction -- public funds -- it is having considered it as a manufacturing method of an electron device provided with a process of combining a group and joining between the 1st electrode and the 2nd electrode, at least.
[0026]In a manufacturing method of an electron device concerning the 5th feature of such this invention, a manufacturing method of an electron device concerning the 4th feature of this invention -- the same -- the 1st liquid phase diffusion metal and the 1st junction -- public funds -- combination temperature with a group -- the 2nd junction -- public funds -- it being able to lower by a group and,

the 2nd liquid phase diffusion metal and the 3rd junction -- public funds -- combination temperature with a group -- the 4th junction -- public funds -- since it can lower by a group, welding temperature between the 1st electrode and the 2nd electrode can be lowered, and a low-temperature degree process can be realized.

[0027]

[Embodiment of the Invention]Hereafter, an embodiment of the invention is described in detail with reference to drawings. "The semiconductor device (semiconductor chip)" concerning an embodiment of the invention, A "substrate", a "semiconductor device", a "semiconductor module", etc. explain the "electron device" which embodies the "electron device" concerning this invention, and is collectively built over this invention while explaining these semiconductor devices concerning an embodiment of the invention.

[0028](A 1st embodiment) A 1st embodiment of this invention explains the example which applied this invention to the semiconductor device (electron device) which adopts ball bonding array structure and adopts a flip chip inner-lead-bonding (only henceforth FC-ILB) method.

[0029][Structure of a semiconductor device] as shown in drawing 2, the semiconductor device 1 which adopts the FC-ILB method concerning a 1st embodiment of this invention, It has the substrate 10, the semiconductor device (semiconductor chip) 20 mounted with FC structure on the substrate 10, the protection resin 30 which protects the semiconductor device 20, and the stiffener 31 which protects the lead wire 11 on the semiconductor device 20 and the substrate 10, and is built. The semiconductor device 1 is provided with the solder ball electrode 41 on the external terminal 12 allocated in the rear face of the substrate 10.

[0030]The TAB tape board which has low heat resistance is used for the substrate 10. As the substrate 10 of the semiconductor device 1 concerning a 1st embodiment of this invention, the polyimide system resin tape substrate which has the heat resistance of the range of 150 ** - 300 **, for example can be used practical. This polyimide system resin tape substrate is provided with moderate flexible nature.

[0031]The lead wire 11 is allocated on the surface of the substrate 10 (figure Nakagami side surface). As shown in drawing 1 (A), the lead wire 11 made the glue line 16 intervene, and is pasted up on the surface of the substrate 10. For example, resin system adhesives can be used for this glue line 16 practical. In the center portion (mount field of the semiconductor device 20) of the substrate 10, the end side of the lead wire 11 is used as the electrode 110. This electrode 110 corresponds to one example of an "electrode", the "1st electrode", or the "2nd electrode" concerning this invention. In the peripheral part of the substrate 10, the other end side of the lead wire 11 is electrically connected to the external terminal 12 of the rear face of the substrate 10 through the connecting hole wiring 13. The lead wire 11 is excellent in electrical conductivity, and can use for example, the Cu foil film which is a liquid phase diffusion metal practical, and this Cu foil film is formed by 20-micrometer thickness. The thing of the lead wire 11 for which grinding treatment, Cu plating processing, etc. are performed in the surface of the electrode 110 at least, and surface roughness Rmax of the electrode 110 is set as 0.2 micrometer or less is preferred (see the 8th embodiment of this invention.). A Cu foil film can be used for the external terminal 12 practical like the lead wire 11, for example. Cu plating film can be used for the connecting hole wiring 13 practical, for example.

[0032]In the substrate 10, the surface side is covered with the solder resist film 14 except for the field of the electrode 110 of the lead wire 11, and the rear-face side is covered with the solder resist film 15 except for the field of the external terminal 12.

[0033]The semiconductor device 20 comprises a silicon single crystal chip in a 1st embodiment of this invention, and the store circuit, the logic circuit, or the integrated circuit that combined them is carried in the principal surface of the semiconductor device 20. Since the FC-IBL method is adopted in the semiconductor device 1 concerning a 1st embodiment of this invention, the semiconductor device 20 is mounted by the facedown method which opposed the principal surface to the surface of the substrate 10. Two or more bonding pads (electrode) 21 connected to the above-mentioned store circuit etc. are allocated in the principal surface of the semiconductor device 20. The bonding pad 21 is formed of the wiring which electrically connects between the circuits of the semiconductor device 20, and between elements, for example, a same conductive layer, for example, an Al film, and aluminum alloy films (aluminum-Si, aluminum-Cu, aluminum-Cu-Si, etc.).

[0034]And in the semiconductor device 1 applied to a 1st embodiment of this invention as shown in drawing 1 (A) and drawing 2, The electrode 110 of the lead wire 11 which has a liquid phase diffusion metal in a surface layer at least, a liquid phase diffusion metal and the 1st junction that this liquid phase diffusion metal is made to combine -- public funds -- a group and a liquid phase diffusion metal, and the 1st junction -- public funds -- the 2nd junction that lowers combination temperature with a group -- public funds -- with the liquid-phase-diffusion-welding layer 56 on the electrode 110 which contains a group at least. Have the gold bump electrode 40 on the liquid-phase-diffusion-welding layer 56, the liquid-phase-diffusion-welding layer 56 and the gold bump electrode 40 are made to intervene, and between the electrode 110 and the bonding pads 21 of the semiconductor device 20 is connected

electrically and mechanically. That is, the semiconductor device 20 is mounted on the substrate 10. The gold bump electrode 40 corresponds to one example of the "2nd electrode" concerning this invention.

[0035]Here, the electrode 110 is formed with the Cu foil film in which the whole is a liquid phase diffusion metal. the 1st junction -- public funds -- Sn can be used for a group practical, for example -- the 2nd junction -- public funds -- Bi can be used for a group practical, for example. therefore, the liquid-phase-diffusion-welding layer 56 concerning a 1st embodiment of this invention -- the 2nd junction -- public funds -- Cu which is the electrode 110 at least in the state where combination temperature was lowered by Bi which is a group, and is a liquid phase diffusion metal, and the 2nd junction -- public funds -- as a result of combining Sn which is a group, it is the generated joining layer. Actually, as shown in drawing 1 (A), the liquid-phase-diffusion-welding layer 56 is constituted by the 1st joining layer 56A that consists of Cu_3Sn on the electrode 110, and the 2nd joining layer 56B that consists of Cu_6Sn_5 on this 1st joining layer 56A.

[0036]Before junction between the electrode 110 of the lead wire 11, and the gold bump electrode 40 who made the liquid-phase-diffusion-welding layer 56 intervene, The 1st metal layer 52 for junction it is allocated on the electrode 110 and combined with a liquid phase diffusion metal as shown in drawing 1 (B), The 2nd metal layer 53 for junction that is allocated on the 1st metal layer 52 for junction, and lowers the combination temperature of a liquid phase diffusion metal and the 1st metal layer 52 for junction is constituted, and the liquid-phase-diffusion-welding layer 56 is generated from this 1st metal layer 52 for junction, and the 2nd metal layer 53 for junction. in a 1st embodiment of this invention, thickness can use Sn plating layer which is 10 micrometers practical for the 1st metal layer 52 for junction -- the 2nd junction -- public funds -- thickness can use Bi plating layer which is 10 micrometers for a group practical.

[0037]If the monolayer of the 1st metal layer 52 for junction (Sn plating layer) is formed on the electrode 110 as shown in drawing 4 (A), and annealing treatment with a temperature of 150 ** is performed to this 1st metal layer 52 for junction, As are shown in drawing 4 (B), and the melting point of Sn shows drawing 4 (C) the 1st metal layer 52 for junction with a solid state for 232 **, liquid phase diffusion arises, and between the electrode 110 and the 1st metal layer 52 for junction, the liquid-phase-diffusion-welding layer 57 is formed. This liquid-phase-diffusion-welding layer 57 is formed of the 1st joining layer 57A that consists of Cu_3Sn, and the 2nd joining layer 57B that consists of Cu_6Sn_5 on this 1st joining layer 57A. As shown in drawing 5, in the 1st joining layer 57A and 2nd joining layer 57B of the liquid-phase-diffusion-welding layer 57, liquid phase diffusion all advances with the increase in the leaving times after annealing treatment, and, as for the generated amount (thickness), the upward tendency is shown.

[0038]As shown in drawing 3 (A), on the electrode 110 On the other hand, the 1st metal layer 52 for junction (Sn plating layer), If the composite layer of the 2nd metal layer 53 for junction (Bi plating layer) is formed and annealing treatment with a same temperature [the / as this 1st metal layer 52 for junction and the 2nd metal layer 53 for junction] of 150 ** is performed, Since the melting point of Sn and Bi falls at 139 ** as shown in drawing 3 (B), in the state of the solution layer 56D of Sn and Bi, as shown in drawing 3 (C), liquid phase diffusion arises, and the liquid-phase-diffusion-welding layer 56 is formed on the electrode 110. This liquid-phase-diffusion-welding layer 56 is formed as mentioned above of the 1st joining layer 56A and the 2nd joining layer 56B on this 1st joining layer 56A. In [as shown in drawing 5] the 1st joining layer 56A and 2nd joining layer 56B of the liquid-phase-diffusion-welding layer 56, Although liquid phase diffusion all advances with the increase in the leaving times after annealing treatment like the 1st joining layer 57A of the liquid-phase-diffusion-welding layer 57, and the 2nd joining layer 57B and the generated amount shows the upward tendency, The generated amount is large about 1.3 to 2.2 times compared with the 1st joining layer 57A and 2nd joining layer 57B. namely, the sum total thickness of the liquid-phase-diffusion-welding layer 56 shown in drawing 3 (C) -- it is thick (a liquid phase diffusing capacity is greatly) -- it means that bonding strength becomes high.

[0039]As shown in drawing 1 (A), the barrier metal layer 55 is made to intervene between the bonding pad 21 of the semiconductor device 20, and the gold bump electrode 40, and it is joined electrically and mechanically. The bipolar membrane of a titanium (Ti) layer and a tungsten (W) layer can be used for this barrier metal layer 55 practical, for example. It can replace with the gold bump electrode 40, and a copper bump electrode etc. can be used.

[0040]As shown in drawing 2, even if there are few semiconductor devices 20, the principal surface (element formation side) is covered with the protection resin 30. For example, polyimide system resin can be used for this protection resin 30 practical.

[0041]In the semiconductor device 1 concerning the 1st feature of this invention constituted in this

way, the welding temperature by the liquid phase diffusion between the electrode 110 and other gold bump electrodes 40 connected to it -- the 2nd junction -- public funds -- lowering by a group (for example, Bi) -- moreover -- the bonding strength between both sides -- the 2nd junction -- public funds, since a group can raise. Heat-resistant temperature, such as parts and material, especially the heat-resistant temperature of the substrate 10 can be lowered. Therefore, to the substrate 10, heat-resistant temperature is low, for example, since it has the heat-resistant temperature of 300 ** or less and the cheap tape base material of copper foil / glue line / polyimide system resin can be used, the product cost of the semiconductor device 1 is reducible.

[0042][Manufacturing method of a semiconductor device] Next, drawing 6 thru/or drawing 13 are used and the manufacturing method of the above-mentioned semiconductor device 1 is explained.

[0043](1) First, as shown in drawing 6, the substrate 10 is prepared. The lead wire 11 is formed on the surface of this substrate 10, and the external terminal 12 electrically connected to the lead wire 11 through the connecting hole wiring 13 is formed on the rear face (refer to drawing 2.). The end side of the lead wire 11 is exposed to the surface side of the substrate 10 as the electrode 110, and the peripheral part of the lead wire 11 is covered with the solder resist film 14. The rear-face top of the substrate 10 is covered with the solder resist film 15 except for the field of the external terminal 12.

[0044](2) As shown in drawing 7, form the 1st metal layer 52 for junction on the surface of the electrode 110 of the lead wire 11. As mentioned above, Sn plating layer can be used for the 1st metal layer 52 for junction practical.

[0045](3) Succeedingly, as shown in drawing 8, form the 2nd metal layer 53 for junction on the 1st metal layer 52 for junction. As mentioned above, Bi plating layer can be used for the 2nd metal layer 53 for junction practical.

[0046](4) Carry out installation maintenance of the semiconductor device 20 by face up on the heating stage 61 in the thermocompression bonding device (refer to drawing 9.) 60. It is in the state where made the barrier metal layer 55 intervene and the gold bump electrode 40 was allocated on the bonding pad 21, in the semiconductor device 20. As shown in drawing 9, between the semiconductor device 20 by which installation maintenance was carried out in the heating stage 61, and the heat pressing tool 62 by which opposite allocation was carried out on the heating stage 61, the electrode 110 is turned to the bottom and positioning arrangement of the substrate 10 is carried out.

[0047](5) Pressurize, while heating the rear face (drawing 10 Nakagami side surface) of the substrate 10 with the heat pressing tool 62, as shown in drawing 10, make the gold bump electrode 40 intervene and carry out thermocompression bonding of between the bonding pad 21 of the semiconductor device 20, and the electrodes 110 of the substrate 10. By liquid phase diffusion which Cu of the electrode 110 and Sn of the 1st metal layer 52 for junction combine in the state where combination temperature was lowered as mentioned above by the 2nd metal layer 53 for junction, at this time. The liquid-phase-diffusion-welding layer 56 is generated between the electrode 110 and the gold bump electrode 40, and between the electrode 110 and the gold bump electrodes 40 is joined electrically and mechanically by this liquid-phase-diffusion-welding layer 56. Each heating preset temperature of the heating stage 61 and the heat pressing tool 62 is set up within the limits of 70 ** - 200 ** in consideration of a fallen part of some (30 ** - 50 **). In such a low temperature requirement, the liquid-phase-diffusion-welding layer 56 can obtain sufficient bonding strength.

[0048](6) As shown in drawing 11, form the protection resin 30 which covers the principal surface of the semiconductor device 20. The protection resin 30 can be formed by being filled up with the polyimide system resin which has mobility through the opening 10H of the center portion of the substrate 10, and stiffening this polyimide system resin with which it filled up, for example by the dropping applying method.

[0049](7) As shown in drawing 12, the semiconductor device 1 concerning a 1st embodiment of this invention can be completed by attaching the stiffener 31 which covers and protects the semiconductor device 20.

[0050](8) The solder ball electrode 41 is formed in the external terminal 12 of the substrate 10 of the semiconductor device 1 after this.

[0051]In the manufacturing method of the semiconductor device 1 concerning a 1st embodiment of such this invention, the combination temperature (liquid phase diffusion temperature) of the liquid phase diffusion metal (Cu) of the electrode 110, and the 1st metal layer 52 for junction (Sn) -- the 2nd junction -- public funds -- since it can lower by the group (Bi) 53, the welding temperature between the electrode 110 and the gold bump electrode 40 can be lowered, and a low-temperature degree process can be realized.

[0052][Modification(s)]

(1) In the semiconductor device 1 concerning a 1st embodiment of above-mentioned this invention, an Au foil film, an Al foil film, a Ni-foils film, etc. can be used for the electrode 110 of the substrate 10 practical as liquid phase diffusion metals other than a Cu foil film.

[0053](2) in the semiconductor device 1 concerning a 1st embodiment of this invention -- junction of the 1st of the 1st metal layer 52 for junction -- public funds -- the duality which makes a group one of Pb, In, or them other than Sn with the main ingredients -- the above alloy is contained at least. for example, the 1st junction -- public funds -- a group -- 97 atom %In-three-atom %Ag and 52 atom %In-48-atom %Sn. 50.9 atom %In-49.1-atom %Sn, 57 atom %Bi-43-atom %Sn, 58 atom %Bi-42-atom %Sn, 55 atom %Bi-45-atom %Pb, 55.5 atom %Bi-44.5-atom %Pb, 33.3 atom %Bi-66.7-atom %In, Quaternary alloys, such as ternary alloy [, such as binary alloys, such as 67 atom %Bi-33-atom %In, 80 atom %In-15-atom %Pb-five atom %Ag, and 46 atom %Bi-34-atom %Sn-20 atom %Pb,] and 49 atom %Bi-21-atom %In-18-atom %Pb-12-atom %Sn, are contained. Gallium (Ga) can be included in the 1st metal layer 52 for junction.

[0054](3) in the semiconductor device 1 concerning a 1st embodiment of this invention -- junction of the 2nd of the 2nd metal layer 53 for junction -- public funds -- the duality which makes a group either [other than Bi] Ag, In or Bi, Ag or In with the main ingredients at least -- the above alloy is contained.

[0055](A 2nd embodiment) A 2nd embodiment of this invention explains the example which applied this invention to the semiconductor device (electron device) which adopts ball bonding array structure and adopts a beam lead inner-lead-bonding (only henceforth BL-ILB) method.

[0056][Structure of a semiconductor device] as shown in drawing 14, the semiconductor device 2 which adopts the BL-ILB method concerning a 2nd embodiment of this invention, It has the substrate 70, the semiconductor device (semiconductor chip) 20 mounted with the beam-lead structure on the substrate 70, the protection resin 32 which protects the semiconductor device 20, and the stiffener 31 which protects the semiconductor device 20, and is built. The semiconductor device 2 is provided with the solder ball electrode 41 on the external terminal 72 allocated in the rear face of the substrate 70.

[0057]The polyimide system resin tape substrate which the TAB tape board which has low heat resistance is used like the semiconductor device 1 concerning a 1st embodiment of this invention, for example, has the heat resistance of the range which are 150 ** - 300 ** can be used for the substrate 70 practical.

[0058]The lead 71 is allocated on the rear face of the substrate 70 (figure Nakashita side surface). Although this lead 71 is not illustrated, it made the glue line 16 intervene like the lead wire 11 shown in drawing 1 (A), and is pasted up on the surface of the substrate 70. In the center portion (mount field of the semiconductor device 20) of the substrate 10, it has the opening 70H, and the end side of the lead 711 is projected by this opening 70H as the electrode (beam lead) 710. This electrode 710 corresponds to one example of an "electrode", the "1st electrode", or the "2nd electrode" concerning this invention. In the peripheral part of the substrate 70, the other end side of the lead 71 is electrically connected to the external terminal 72. The electrode 710 constituted by the lead 71 and it in one is excellent in electrical conductivity, and can use for example, the Cu foil film which is a liquid phase diffusion metal practical, and this Cu foil film is formed by 20-micrometer thickness. Surface roughness Rmax of the electrode 710 has a preferred thing of the lead 71 which grinding treatment, Cu plating processing, etc. are performed in the surface of the electrode 710 at least, and is set as 0.2 micrometer or less. A Cu foil film can be used for the external terminal 72 practical like the lead 71, for example.

[0059]In the substrate 70, the rear-face side is covered with the solder resist film 74 except for the field of the electrode 710 of the lead 71.

[0060]The semiconductor device 20 is the same as the semiconductor device 20 concerning a 1st embodiment of this invention, and is mounted by the facedown method which opposed the principal surface to the surface of the substrate 70. Two or more bonding pads (electrode) 21 are allocated in the principal surface of the semiconductor device 20.

[0061]And in the semiconductor device 2 applied to a 2nd embodiment of this invention as shown in drawing 14 and drawing 15, The electrode 710 of the lead 71 which has a liquid phase diffusion metal (for example, Cu) in a surface layer at least like the semiconductor device 1 concerning a 1st embodiment of this invention, a liquid phase diffusion metal and the 1st junction that this liquid phase diffusion metal is made to combine -- public funds -- a group (for example, Sn). and a liquid phase diffusion metal and the 1st junction -- public funds -- the 2nd junction that lowers combination temperature with a group -- public funds -- with the liquid-phase-diffusion-welding layer 56 on the electrode 710 which contains a group (for example, Bi) at least. Have the gold bump electrode 40 on the liquid-phase-diffusion-welding layer 56, the liquid-phase-diffusion-welding layer 56 and the gold bump electrode 40 are made to intervene, and between the electrode 710 and the bonding pads 21 of the semiconductor device 20 is connected electrically and mechanically. The liquid-phase-diffusion-welding layer 56 is constituted in practice by the 1st joining layer 56A that consists of Cu_3Sn on the electrode 710, and the 2nd joining layer 56B that consists of Cu_6Sn_5 on this 1st joining layer 56A.

[0062]The barrier metal layer 55 is intervened between the bonding pad 21 of the semiconductor

device 20, and the gold bump electrode 40, and it is joined electrically and mechanically. As shown in drawing 14, even if there are few semiconductor devices 20, the principal surface (element formation side) is covered with the protection resin 32. For example, polyimide system resin can be used for this protection resin 32 practical.

[0063]In the semiconductor device 2 concerning the 2nd feature of this invention constituted in this way, the welding temperature by the liquid phase diffusion between other gold bump electrodes 40 connected with the electrode 710 like the semiconductor device 1 concerning a 1st embodiment of this invention at it -- the 2nd junction -- public funds -- it lowering by a group (for example, Bi), and, moreover -- the bonding strength between both sides -- the 2nd junction -- public funds -- since a group can raise, heat-resistant temperature, such as parts and material, especially the heat-resistant temperature of the substrate 70 can be lowered. Therefore, to the substrate 70, heat-resistant temperature is low, for example, since it has the heat-resistant temperature of 300 ** or less and the cheap tape base material of copper foil / glue line / polyimide system resin can be used, the product cost of the semiconductor device 2 is reducible.

[0064][Manufacturing method of a semiconductor device] Next, the manufacturing method of the semiconductor device 2 concerning a 2nd embodiment of this invention is explained using drawing 16 and drawing 17.

[0065](1) The manufacturing method of the semiconductor device 2 concerning a 2nd embodiment of this invention, Like [although not illustrated] the manufacturing method of the semiconductor device 1 concerning a 1st embodiment of this invention, The substrate 70 is prepared first and each of the 1st metal layer 52 for junction (for example, Sn) and the 2nd metal layer 53 for junction (for example, Bi) is formed one by one on the surface of the electrode (beam lead) 710 of the lead 71 of the substrate 70.

[0066](2) Carry out installation maintenance of the semiconductor device 20 by face up on the heating stage 61 in the thermocompression bonding device (refer to drawing 16.) 60. It is in the state where made the barrier metal layer 55 intervene and the gold bump electrode 40 was allocated on the bonding pad 21, in the semiconductor device 20. As shown in drawing 16, positioning arrangement of the substrate 70 is carried out between the heat pressing tools 62 by which opposite allocation was carried out on the semiconductor device 20 which laid in the heating stage 61 and was held, and the heating stage 61. By this positioning arrangement, the gold bump electrode 40 is made to intervene on the bonding pad 21 of the semiconductor device 20, and the electrode 710 of the substrate 70 is positioned.

[0067](3) Pressurize, while heating the rear face (drawing 17 Nakagami side surface) of the electrode 710 of the substrate 70 with the heat pressing tool 62, as shown in drawing 17, make the gold bump electrode 40 intervene and carry out thermocompression bonding of between the bonding pad 21 of the semiconductor device 20, and the electrodes 710 of the substrate 70. By liquid phase diffusion which Cu of the electrode 710 and Sn of the 1st metal layer 52 for junction combine in the state where combination temperature was lowered as mentioned above by the 2nd metal layer 53 for junction, at this time. The liquid-phase-diffusion-welding layer 56 is generated between the electrode 710 and the gold bump electrode 40, and between the electrode 710 and the gold bump electrodes 40 is joined electrically and mechanically by this liquid-phase-diffusion-welding layer 56. Each heating preset temperature of the heating stage 61 and the heat pressing tool 62 is set up within the limits of 70 ** - 200 **. In such a low temperature requirement, the liquid-phase-diffusion-welding layer 56 can obtain sufficient bonding strength.

[0068](4) Form the protection resin 32 which covers the principal surface of the semiconductor device 20 (refer to drawing 14.). The protection resin 32 can be formed by being filled up with the polyimide system resin which has mobility through the opening 70H of the center portion of the substrate 70, and stiffening this polyimide system resin with which it filled up, for example by the dropping applying method.

[0069](5) By attaching the stiffener 31 which covers and protects the semiconductor device 20, the semiconductor device 2 concerning a 2nd embodiment of this invention can be completed (refer to drawing 14.).

[0070](6) The solder ball electrode 41 is formed in the external terminal 72 of the substrate 70 of the semiconductor device 2 after this.

[0071]In the manufacturing method of the semiconductor device 2 concerning a 2nd embodiment of such this invention, the combination temperature (liquid phase diffusion temperature) of the liquid phase diffusion metal (Cu) of the electrode 710, and the 1st metal layer 52 for junction (Sn) -- the 2nd junction -- public funds -- since it can lower by the group (Bi) 53, the welding temperature between the electrode 710 and the gold bump electrode 40 can be lowered, and a low-temperature degree process can be realized.

[0072](A 3rd embodiment) A 3rd embodiment of this invention explains the example which applied this invention to the semiconductor device (electron device) which adopts resin-mould structure.

[0073]As shown in drawing 18, the semiconductor device 3 concerning a 3rd embodiment of this invention, The tab (tab lead) 80A and the semiconductor device 20 mounted by the face-up method on this tab 80A, It has the resin sealed portion 82 which carries out the hermetic seal of the inner lead of the lead 80B for which the inner lead was electrically connected to the bonding pad 21 of the semiconductor device 20 through the bonding wire 81, and the tab 80A, the semiconductor device 20 and the lead 80B, and is built.

[0074]In a 3rd embodiment of this invention, in the manufacturing process (assembly process) of the semiconductor device 3, what was formed in the same leadframe in one is cut from the frame of a leadframe, and the tab 80A and the lead 80B mold it. Cu board, a Cu alloy board, an iron nickel (Fe-nickel) alloy plate, etc. excellent in electrical conductivity can be used for this tab 80A and lead 80B practical, for example. What formed with the iron nickel alloy on the whole, and formed Cu cladding layer in the surface layer of the tab 80A at least may be used for the tab 80A and the lead 80B.

[0075]The semiconductor device 20 makes the liquid-phase-diffusion-welding layer 56 intervene, and is joined to the tab 80A. The 1st joining layer 56A that consists of Cu_3Sn on the tab 80A like the semiconductor device 1 concerning a 1st embodiment of above-mentioned this invention as for the liquid-phase-diffusion-welding layer 56, It has the 2nd joining layer 56B that consists of Cu_6Sn_5 on this 1st joining layer 56A, and the 3rd joining layer 56C that consists of Cu_3Sn on the 2nd joining layer 56B further, and is constituted. In [as shown in drawing 19] before [before mount of a up to / the tab 80A of the semiconductor device 20] liquid phase diffusion treatment, the tab 80A top -- the liquid phase diffusion metal layer 54A, the 1st metal layer 52A for junction, and the 2nd junction -- public funds -- each of the group 53A is formed one by one, and each of the liquid phase diffusion metal layer 54B, the 3rd metal layer 52B for junction, and the 4th metal layer 53B for junction is formed one by one on the rear face of the semiconductor device 20. In the semiconductor device 3 concerning a 3rd embodiment of this invention, for example, Cu plating layer which is a liquid phase diffusion metal can be used for each of the liquid phase diffusion metal layers 54A and 54B practical. Sn plating layer can be used for each of the 1st metal layer 52A for junction, and the 3rd metal layer 52B for junction practical like the 1st metal layer 52 for junction of the semiconductor device 1 concerning a 1st embodiment of this invention. Bi plating layer can be used for the 2nd metal layer 53A for junction, and the 4th metal layer 53B for junction practical like the 2nd metal layer 53 for junction of the semiconductor device 1 concerning a 1st embodiment of this invention.

[0076]For example at the temperature of 150 ** - 200 **, liquid phase diffusion treatment by heating for 10 seconds, After combination temperature has been lowered by the 2nd metal layer 53A for junction, the liquid phase diffusion metal layer 54A on the tab 80A and the 1st metal layer 52A for junction are combined, A part of 1st joining layer 56A and 2nd joining layer 56B are generable, After combination temperature has been lowered by the 4th metal layer 53B for junction, the liquid phase diffusion metal layer 54B on the rear face of the semiconductor device 20 and the 3rd metal layer 52B for junction are combined, A part of 3rd joining layers 56C and 2nd remaining joining layers 56B can be generated, and the liquid-phase-diffusion-welding layer 56 can be formed.

[0077]About the modification of each material of the liquid phase diffusion metal layers 54A and 54B, the 1st metal layer 52A for junction, the 2nd metal layer 53A for junction, the 3rd metal layer 52B for junction, and the 4th metal layer 53B for junction, it is the same as that of the modification explained with the semiconductor device 1 concerning a 1st embodiment of this invention.

[0078]In the semiconductor device 3 concerning a 3rd embodiment of this invention, it is electrically connected between the semiconductor device 20 and the tab 80A, For example, the tab 80A is used for the semiconductor device 20 also as an "electrode" which supplies a board power supply, and the rear face of the semiconductor device 20 is used also as an "electrode" which receives supply of this board power supply.

[0079]An Au wire, Cu wire, an Al wire, etc. can be used for the bonding wire 81 practical, for example.

[0080]Thermosetting epoxy system resin can be used for the resin sealed portion 82 practical, and this resin sealed portion 82 is formed by the transfermold method.

[0081]In the semiconductor device 3 concerning the 3rd feature of this invention constituted in this way, Like each of the semiconductor device 1 concerning a 1st embodiment of this invention, and the semiconductor device 2 concerning a 2nd embodiment of this invention, other semiconductor devices 20 (a silicon single crystal substrate.) connected with the tab (electrode) 80A at it The welding temperature by the liquid phase diffusion between electrodes can be lowered by the 2nd metal layer 53A for junction (for example, Bi), and the 4th metal layer 53B for junction, and, moreover, the 2nd metal layer 53A for junction and the 4th metal layer 53B for junction can raise the bonding strength between both sides. Therefore, the temperature of the thermocompression bonding in the case of mounting the semiconductor device 20 on the tab 80A can be set as the degree of low temperature of 300 ** or less, and it can mount in a short time extremely. When resin adhesive was used, 1 hour - 3

hours were needed for mount, but in the semiconductor device 3 concerning a 3rd embodiment of this invention, it can mount within the limits of tens of seconds. Since the liquid-phase-diffusion-welding layer 56 between the semiconductor device 20 and the tab 80A is excellent in thermal conductivity, the high semiconductor device 3 of a radiation effect is realizable.

[0082](A 4th embodiment) A 4th embodiment of this invention explains the example which applied this invention to the semiconductor device (electron device) which adopts ball bonding array structure.

[0083]As shown in drawing 20, the semiconductor device 4 which adopts the ball bonding array structure concerning a 4th embodiment of this invention is provided with the substrate 90 and the semiconductor device (semiconductor chip) 20 mounted by FC method on the substrate 90, and is built. The semiconductor device 4 is provided with the solder ball electrode 41 on the external terminal 92 allocated in the rear face of the substrate 90.

[0084]An epoxy-system-resin board, a ceramics board, etc. can be used for the substrate 90 practical. The lead wire 91 is allocated on the surface of the substrate 90 (figure Nakagami side surface). Although this lead wire 91 is not illustrated, it made the glue line intervene like the lead wire 11 shown in drawing 1 (A), and is pasted up on the surface of the substrate 90. The connection section with the semiconductor device 20 of the lead wire 91 is used as the electrode 910. This electrode 910 corresponds to one example of an "electrode", the "1st electrode", or the "2nd electrode" concerning this invention. The lead wire 91 is electrically connected to the external terminal 92 through the connecting hole wiring 93 which penetrates the substrate 91. The electrode 910 constituted by the lead wire 91 and it in one is excellent in electrical conductivity, and can use for example, the Cu foil film which is a liquid phase diffusion metal practical, and this Cu foil film is formed by 20-micrometer thickness. Surface roughness Rmax of the electrode 910 has a preferred thing of the lead wire 91 which grinding treatment, Cu plating processing, etc. are performed in the surface of the electrode 910 at least, and is set as 0.2 micrometer or less. A Cu foil film can be used for the external terminal 92 practical like the lead wire 91, for example.

[0085]The semiconductor device 20 is the same as the semiconductor device 20 concerning a 1st embodiment of this invention, and a 2nd embodiment of this invention, and is mounted by the facedown method which opposed the principal surface to the surface of the substrate 90. Two or more bonding pads (electrode) 21 are allocated in the principal surface of the semiconductor device 20.

[0086]And in the semiconductor device 4 concerning a 4th embodiment of this invention, The electrode 910 of the lead wire 91 which has a liquid phase diffusion metal (for example, Cu) in a surface layer at least like the semiconductor device 1 concerning a 1st embodiment of this invention, a liquid phase diffusion metal and the 1st junction that this liquid phase diffusion metal is made to combine -- public funds -- a group (for example, Sn). and a liquid phase diffusion metal and the 1st junction -- public funds -- the 2nd junction that lowers combination temperature with a group -- public funds -- with the liquid-phase-diffusion-welding layer 56 on the electrode 910 which contains a group (for example, Bi) at least. Have the copper bump electrode 42 on the liquid-phase-diffusion-welding layer 56, the liquid-phase-diffusion-welding layer 56 and the copper bump electrode 42 are made to intervene, and between the electrode 910 and the bonding pads 21 of the semiconductor device 20 is connected electrically and mechanically. The liquid-phase-diffusion-welding layer 56 like the semiconductor device 3 concerning a 3rd embodiment of this invention in practice, It is constituted by the 1st joining layer 56A that consists of Cu_3Sn on the electrode 910, the 2nd joining layer 56B that consists of Cu_6Sn_5 on this 1st joining layer 56A, and the 3rd joining layer 56C that consists of Cu_3Sn on the 2nd joining layer 56B further.

[0087]In [as shown in drawing 21] before [before the mount to the substrate 90 of the semiconductor device 20] liquid phase diffusion treatment, the lead wire 91 -- at least -- the electrode 910 top -- the 1st metal layer 52A for junction, and the 2nd junction -- public funds -- each of the group 53A is formed one by one, and each of the 3rd metal layer 52B for junction and the 4th metal layer 53B for junction is formed one by one on the copper bump electrode 42. The surface of the copper bump electrode 42 performs grinding treatment, Cu plating processing, etc. beforehand, and, as for surface roughness Rmax of the electrode 910, being set as 0.2 micrometer or less is preferred. In the semiconductor device 4 concerning a 4th embodiment of this invention, Sn plating layer can be used for each of the 1st metal layer 52A for junction, and the 3rd metal layer 52B for junction practical like the 1st metal layer 52 for junction of the semiconductor device 1 concerning a 1st embodiment of this invention. Bi plating layer can be used for the 2nd metal layer 53A for junction, and the 4th metal layer 53B for junction practical like the 2nd metal layer 53 for junction of the semiconductor device 1 concerning a 1st embodiment of this invention.

[0088]For example at the temperature of 150 ** - 200 **, liquid phase diffusion treatment by heating for 10 seconds, After combination temperature has been lowered by the 2nd metal layer 53A for junction, the liquid phase diffusion metal (Cu) of the electrode 910 and the 1st metal layer 52A for junction are combined, A part of 1st joining layer 56A and 2nd joining layer 56B are generable, By the

4th metal layer 53B for junction, where combination temperature is lowered, the liquid phase diffusion metal of the copper bump electrode 42 and the 3rd metal layer 52B for junction can be combined, a part of 3rd joining layers 56C and 2nd remaining joining layers 56B can be generated, and the liquid-phase-diffusion-welding layer 56 can be formed.

[0089]About the modification of each material of the 1st metal layer 52A for junction, the 2nd metal layer 53A for junction, the 3rd metal layer 52B for junction, and the 4th metal layer 53B for junction, it is the same as that of the modification explained with the semiconductor device 1 concerning a 1st embodiment of this invention.

[0090]The barrier metal layer 55 is intervened between the bonding pad 21 of the semiconductor device 20, and the copper bump electrode 42, and it is joined electrically and mechanically.

[0091]In the semiconductor device 4 concerning the 4th feature of this invention constituted in this way, the welding temperature by the liquid phase diffusion between other copper bump electrodes 42 connected with the electrode 910 like the semiconductor device 1 concerning a 1st embodiment of this invention at it -- the 2nd junction -- public funds -- a group and the 4th junction -- public funds -- it lowering by a group (for example, Bi), and, moreover -- the bonding strength between both sides -- the 2nd junction -- public funds -- a group and the 4th junction -- public funds -- since a group can raise, heat-resistant temperature, such as parts and material, can be lowered. Therefore, a low-temperature degree process 300 ** or less is employable. In the semiconductor device 4 especially applied to a 4th embodiment of this invention, Since liquid phase diffusion treatment can be performed at a temperature lower than the melting point of this solder ball electrode 41 after forming the solder ball electrode (for example, melting point temperature of 180 **) 41 in the external terminal 92 of the substrate 90, bonding of the semiconductor device 20 can be carried out to the substrate 90.

[0092](A 5th embodiment) A 5th embodiment of this invention, It is an application of the semiconductor device 4 concerning a 4th embodiment of this invention, and the example which applied this invention to the semiconductor module (electron device) which adopted ball bonding array structure and laminated two or more semiconductor devices is explained.

[0093]As shown in drawing 22, on the substrate 90 and the substrate 90, the semiconductor module 5 which adopts the ball bonding array structure concerning a 5th embodiment of this invention is provided with two or more semiconductor devices (semiconductor chip) 201-204 by which three-dimensional lamination was carried out, and is built. Although the semiconductor module 5 concerning a 5th embodiment of this invention explains the example for which the four semiconductor devices 201-204 were laminated, the lamination number is not limited to four pieces, for example, eight pieces, 16 laminations, etc. are possible for it. The semiconductor module 5 is provided with the solder ball electrode 41 on the external terminal 92 allocated in the rear face of the substrate 90.

[0094]A thing equivalent to the substrate 90 of the semiconductor device 4 concerning a 4th embodiment of this invention can be used for the substrate 90.

[0095]Although the semiconductor devices 201-204 are the same as the semiconductor device 20 concerning a 1st embodiment of this invention thru/or a 4th embodiment of this invention fundamentally, The penetration copper bump electrode 421 penetrated at the rear face from the bonding pad 21 of the surface (principal surface) is allocated by the semiconductor device 201, Similarly, the penetration copper bump electrode 423 is allocated by the semiconductor device 203, and the penetration copper bump electrode 424 is allocated in the semiconductor device 204 for the penetration copper bump electrode 422 by the semiconductor device 202, respectively. The penetration copper bump electrode 421 can form a breakthrough in the semiconductor device 201 by laser beam machining, for example, and can form it by laying under this breakthrough. The surface side of the semiconductor device 201 of the penetration copper bump electrode 421 is used as the projected electrode 421A, and is used as the electrode 421B which also projected the rear-face side. Similarly, the surface side of the semiconductor device 202 of the penetration copper bump electrode 422 is used as the electrode 422A, and the rear-face side is used as the electrode 422B. The surface side of the semiconductor device 203 of the penetration copper bump electrode 423 is used as the electrode 423A, and the rear-face side is used as the electrode 423B. The surface side of the semiconductor device 204 of the penetration copper bump electrode 424 is used as the electrode 424A, and the rear-face side is used as the electrode 424B.

[0096]It excels in electrical conductivity and Cu prism which is a liquid phase diffusion metal can be used for each of these penetration copper bump electrodes 421-424 practical. The electrodes 421A and 421B of the penetration copper bump electrode 421, the electrode 422A of the penetration copper bump electrode 422, Each surface of the electrodes 423A and 423B of 422B and the penetration copper bump electrode 423 and the electrodes 424A and 424B of the penetration copper bump electrode 424 performs grinding treatment, Cu plating processing, etc. beforehand, and, as for surface roughness Rmax, being set as 0.2 micrometer or less is preferred. In the semiconductor device 201, since the surface side is equipped with the electrode 421A and the rear-face side is equipped with the electrode 421B, also in any of a face-up method and a facedown method, bonding can be carried out

on the substrate 90. The same may be said of the other semiconductor devices 202-204.
[0097]And in the semiconductor module 5 concerning a 5th embodiment of this invention, The electrode 910 of the lead wire 91 which has a liquid phase diffusion metal (for example, Cu) in a surface layer at least like the semiconductor device 4 concerning a 4th embodiment of this invention, a liquid phase diffusion metal and the 1st junction that this liquid phase diffusion metal is made to combine -- public funds -- a group (for example, Sn). and a liquid phase diffusion metal and the 1st junction -- public funds -- the 2nd junction that lowers combination temperature with a group -- public funds -- a group (for example, Bi) is included at least. Have the liquid-phase-diffusion-welding layer 56 on the electrode 910, this liquid-phase-diffusion-welding layer 56 is made to intervene, and between the electrode 910 and the electrodes 421B of the semiconductor device 201 is connected electrically and mechanically. The liquid-phase-diffusion-welding layer 56 like the semiconductor device 4 concerning a 4th embodiment of this invention in practice, It is constituted by the 1st joining layer 56A that consists of Cu_3Sn on the electrode 910, the 2nd joining layer 56B that consists of Cu_6Sn_5 on this 1st joining layer 56A, and the 3rd joining layer 56C that consists of Cu_3Sn on the 2nd joining layer 56B further.
[0098]In before [before the bonding to the substrate 90 of the semiconductor device 201] liquid phase diffusion treatment, Even if there are few lead wires 91, on the electrode 910 The 1st metal layer 52A for junction, Each of the 2nd metal 53A for junction is formed one by one, and each of the 3rd metal layer 52B for junction and the 4th metal layer 53B for junction is formed one by one on the electrode 421B of the semiconductor device 201 (refer to drawing 21.). For example at the temperature of 150 ** - 200 **, liquid phase diffusion treatment by heating for 10 seconds, After combination temperature has been lowered by the 2nd metal layer 53A for junction, the liquid phase diffusion metal (Cu) of the electrode 910 and the 1st metal layer 52A for junction are combined, A part of 1st joining layer 56A and 2nd joining layer 56B are generable, After combination temperature has been lowered by the 4th metal layer 53B for junction, the liquid phase diffusion metal (Cu) of the electrode 421B and the 3rd metal layer 52B for junction are combined, A part of 3rd joining layers 56C and 2nd remaining joining layers 56B can be generated, and the liquid-phase-diffusion-welding layer 56 can be formed.
[0099]Similarly Between the electrode 421A of the semiconductor device 201, and the electrodes 422B of the semiconductor device 202, Between the electrode 422A of the semiconductor device 202, and the electrode 423B of the semiconductor device 203, all between the electrode 423A of the semiconductor device 203 and the electrode 424B of the semiconductor device 204 make the liquid-phase-diffusion-welding layer 56 intervene, and are connected electrically and mechanically.
[0100]In the semiconductor module 5 concerning the 5th feature of this invention constituted in this way, Between the electrodes 421B of the semiconductor device 201 connected to the electrode 910 and it like the semiconductor device 4 concerning a 4th embodiment of this invention, Between the electrode 421A of the semiconductor device 201, and the electrodes 422B of the semiconductor device 202, Between the electrode 422A of the semiconductor device 202, and the electrodes 423B of the semiconductor device 203, the welding temperature by the liquid phase diffusion between the electrode 423A of the semiconductor device 203, and the electrode 424B of the semiconductor device 204 -- the 2nd junction -- public funds -- a group and the 4th junction -- public funds -- lowering by a group (for example, Bi) -- moreover -- the bonding strength between both sides -- the 2nd junction -- public funds -- a group and the 4th junction -- public funds -- a group can raise. Therefore, a low-temperature degree process 300 ** or less is employable. In the semiconductor module 5 especially applied to a 5th embodiment of this invention, Since liquid phase diffusion treatment can be performed at a temperature lower than the melting point of this solder ball electrode 41 after forming the solder ball electrode 41 in the external terminal 92 of the substrate 90, bonding of the semiconductor devices 201-204 can be carried out to the substrate 90. Since liquid phase diffusion treatment can carry out at a low temperature, the remaining stress between each of the semiconductor devices 201-204 can be decreased.
[0101](A 6th embodiment) A 6th embodiment of this invention explains the semiconductor module (electron device) which combined the semiconductor device 4 concerning a 4th embodiment of this invention, and the semiconductor module 5 concerning a 5th embodiment of this invention.
[0102]As shown in drawing 23, on the substrate 90 and the substrate 90, by FC method, the semiconductor module 6 concerning a 6th embodiment of this invention carries out three-dimensional lamination of two or more semiconductor devices 4 provided with the semiconductor device (semiconductor chip) 20 by which bonding was carried out, and is built. Although the semiconductor module 6 concerning a 6th embodiment of this invention explains the example for which the two semiconductor devices 4 were laminated, the lamination number is not limited to two pieces, for example, four pieces, eight pieces, 16 laminations, etc. are possible for it. The external terminal 92 allocated in the rear face of the substrate 90 of the semiconductor device 4 of the bottom of the heap in the semiconductor module 6 is equipped with the solder ball electrode 41.

[0103]Although the liquid-phase-diffusion-welding layer 56 and the copper bump electrode 42 are made to intervene like the semiconductor device 4 concerning a 4th embodiment of this invention between the substrate 90 of the semiconductor device 4 of the semiconductor module 6, and the semiconductor device 20 and it is connected, It is connected electrically and mechanically by the intermediate wiring board 900 between the semiconductor devices 4 laminated up and down.
[0104]The intermediate wiring board 900 equips with the electrode 901 the surface of the substrate formed, for example with a material equivalent to the substrate 90 of the semiconductor device 4, a rear face is equipped with the electrode 902, and it is electrically connected by the connecting hole wiring 903 between the electrodes 901 and 902. Each thing [equipping a surface layer at least with a liquid phase diffusion metal] of the electrodes 901 and 902 is preferred, and each of the electrodes 901 and 902 is formed by the Cu foil film in a 6th embodiment of this invention.
[0105]Between the electrode 911 of the substrate 90 of the semiconductor device 4, and the electrodes 902 by the side of the rear face of the intermediate wiring board 900, It is connected electrically and mechanically by the liquid-phase-diffusion-welding layer 56 and the same liquid-phase-diffusion-welding layer 58 between each of the external terminal (electrode) 92 of the electrode 901 by the side of the surface of the intermediate wiring board 900, and the substrate 90 of the semiconductor device 4.
[0106]In the semiconductor module 6 concerning the 6th feature of this invention constituted in this way, Between the electrodes 902 of the intermediate wiring board 900 connected to the electrode 911 of the substrate 90 of the semiconductor device 4, and it like the semiconductor module 5 concerning a 5th embodiment of this invention, The welding temperature by the liquid phase diffusion between the electrode 901 of the intermediate wiring board 900, and the external terminal 92 of the substrate 90 of the semiconductor device 4, the 2nd junction -- public funds -- a group and the 4th junction -- public funds -- lowering by a group (for example, Bi) -- moreover -- the bonding strength between both sides -- the 2nd junction -- public funds -- a group and the 4th junction -- public funds -- a group can raise. Therefore, a low-temperature degree process 300 ** or less is employable.
[0107](A 7th embodiment) In the semiconductor device 1 concerning a 1st embodiment of this invention, a 7th embodiment of this invention explains the example which can raise further the bonding strength between the electrode 110 of the substrate 10, and the gold bump electrode 40.
[0108]In the semiconductor device 1 concerning a 1st embodiment of this invention, even if a 7th embodiment of this invention has few lead wires 11 on the substrate 10, it carries out flattening of the surface of the electrode 110, i.e., the formation surface of the liquid-phase-diffusion-welding layer 56, before liquid phase diffusion treatment. As shown in drawing 24, flattening (the numerals F show a flattening field.) of the surface of this electrode 110 can be performed by the dent by the heat pressing tool 62 of the thermocompression bonding device 60. As for the electrode contact surface of the heat pressing tool 62, it is preferred to perform mirror finish, for example, as for surface roughness Rmax of the electrode 110, generating to 0.2 micrometer or less is preferred.
[0109]According to the fundamental research which this invention person carried out, surface roughness Rmax of copper foil 1.6 micrometers, As opposed to the welding temperature of liquid phase diffusion treatment having set at 400 **, the junction load having set under the condition of 50MPa for 10 seconds in the jointing time, and the liquid-phase-diffusion-welding layer having been generated by a thickness of about 3 micrometers, In the welding temperature of 0.2 micrometer and liquid phase diffusion treatment, 300 ** and a jointing time were able to set at 10 seconds, the junction load was able to set under the condition of 50MPa, and surface roughness Rmax of copper foil was able to generate the liquid-phase-diffusion-welding layer by a thickness of about 1 micrometer. Namely, the more it makes surface roughness of copper foil small like the latter to the former conditions, the more in the degree of low temperature, a liquid-phase-diffusion-welding layer is thickly generable.
[0110]Directly, flattening of the electrode 110 may go to the surface of a liquid phase diffusion metal, and after forming each of the 1st metal layer 52 for junction, and the 2nd metal layer 53 for junction on the surface of the electrode 110 (after plating), it may be performed. Flattening may be carried out in the state where the pattern NlNGU resist film and protection resist film of the electrode 110 are formed, for example on the electrode 110.
[0111]Thus, in the semiconductor device 1 concerning a 7th embodiment of this invention, While being able to thicken junction thickness of the liquid-phase-diffusion-welding layer 56 and being able to improve bonding strength by carrying out flattening of the surface of the electrode 110 which forms the liquid-phase-diffusion-welding layer 56, liquid phase diffusion temperature can be lowered and low temperature process-ization can be realized.
[0112](An 8th embodiment) An 8th embodiment of this invention, the semiconductor device 1 concerning a 1st embodiment of this invention -- or. In the semiconductor device 4 concerning a 4th embodiment of this invention, the semiconductor module 5 concerning a 5th embodiment of this invention, the semiconductor module 6 concerning a 6th embodiment of this invention, and the

semiconductor device 1 concerning a 7th embodiment of this invention, the example which raised further each bonding strength of the liquid-phase-diffusion-welding layers 56 and 58 is explained -- it has come out.

[0113]An 8th embodiment of this invention is having used the liquid phase diffusion metal of the electrode 110 grade of the substrate 10 of the semiconductor device 1 as the rolling thin film (rolling foil film). A rolling thin film is a thin film which performed the rolling process to the liquid phase diffusion metal, for example, the rolling Cu foil film has the character recrystallized in the range with a particle diameter of 1 micrometer - 20 micrometers in the degree of low temperature of 100 ** - 300 **. This rolling Cu foil film has big particle diameter size compared with the particle diameter of the recrystallization of for example, an electrolysis Cu foil film.

[0114]Drawing 25 shows the relation between the welding temperature of liquid phase diffusion treatment, and the bonding strength of a liquid-phase-diffusion-welding layer. Data (A) is the characteristic of the liquid-phase-diffusion-welding layer which formed each of Sn (1st junction public funds group) of 4-micrometer thickness, and Bi (2nd junction public funds group) of 1 micrometer of thickness on the rolling Cu foil film, and generated Bi(s) mutually where facing each other and rolling Cu foil films are piled up among drawing 25. A jointing time is 10 seconds and junction loads are 50MPa. The following and this condition are the same. Data (B) is the characteristic of the liquid-phase-diffusion-welding layer which formed each of Sn of 4-micrometer thickness, and Bi of 1 micrometer of thickness on the electrolysis Cu foil film, and generated Bi(s) mutually where facing each other and electrolysis Cu foil films are piled up. Compared with data (B), welding temperature also becomes low and, also in bonding strength, the direction of the liquid-phase-diffusion-welding layer generated with data (A), i.e., a rolling Cu foil film, becomes tens times higher from several times. Although the bonding strength of about 300 ** or less becomes zero in the liquid-phase-diffusion-welding layer especially generated by the electrolysis Cu foil film, sufficient bonding strength can be obtained in the liquid-phase-diffusion-welding layer generated by the rolling Cu foil film.

[0115]Each of Sn of 4-micrometer thickness and Bi of 1 micrometer of thickness is formed on a rolling Cu foil film at drawing 25. The characteristic of the liquid-phase-diffusion-welding layer generated where Au (it is equivalent to the gold bump electrode 40) is laid on top of this Bi is used as data (a), Each of Sn of 4-micrometer thickness and Bi of 1 micrometer of thickness is formed on an electrolysis Cu foil film, and the characteristic of the liquid-phase-diffusion-welding layer generated where Au is laid on top of this Bi is shown as data (b). Similarly compared with data (b), those [layer / which was generated by data (a), i.e., a rolling Cu foil film, and Au / liquid-phase-diffusion-welding] can be in welding temperature low, and high bonding strength can be obtained in the range. In particular, at the welding temperature of 260 ** or less, the bonding strength of the liquid-phase-diffusion-welding layer shows the tendency to go up.

[0116]In the semiconductor device or semiconductor module (electron device) concerning an 8th embodiment of this invention constituted in this way, Since particle diameter size of a liquid phase diffusion metal can be enlarged and a plane-of-composition product can be increased by having used the liquid phase diffusion metal as the rolling thin film, the bonding strength of a liquid-phase-diffusion-welding layer can be improved. The liquid-phase-diffusion-welding layer can obtain high bonding strength in the degree of low temperature.

[0117](Other embodiments) Although two or more above-mentioned embodiments indicated this invention, if this invention is limited, he should not understand the statement and the drawing which make a part of this indication. Various alternative embodiments, an example, and an investment technique will become clear [to a person skilled in the art] from this indication.

[0118]For example, the electron device which mounts the semiconductor device 1 grade which requires this invention for a 1st embodiment of this invention on mounting boards, such as a mother board and a daughter board, It is applicable to the electron device etc. which mount the semiconductor module 6 concerning a 6th embodiment of the semiconductor module 5 applied on the above-mentioned mounting board at a 5th embodiment of this invention, or this invention. A liquid-phase-diffusion-welding layer is used for these mounting.

[0119]This invention can be applied, not only when using a liquid-phase-diffusion-welding layer for inter-electrode junction but when forming a liquid-phase-diffusion-welding layer on the substrate which has at least ceramics (aluminum$_2$O$_3$) which are liquid phase diffusion metals, for example in a surface layer and joining electronic parts etc.

[0120]Thus, as for this invention, it is needless to say that various embodiments etc. which have not been indicated here are included. Therefore, the technical scope of this invention is appointed only by the invention specific matter concerning the above-mentioned appropriate claim.

[0121]

[Effect of the Invention]This invention can provide the electron device which has a joinable electrode

in the degree of low temperature.
[0122]This invention can provide the electron device which can decrease product cost by use of the parts which do not need heat resistance, material, etc.
[0123]The electron device whose joined part of an electrode can be electric and which this invention can improve the bonding strength of an electrode, and can improve mechanical reliability can be provided.
[0124]This invention can provide the manufacturing method of the electron device which can make inter-electrode junction the degree of low temperature.
[0125]This invention can provide the manufacturing method of the electron device which can decrease a manufacturing cost.

[Translation done.]